April 1996



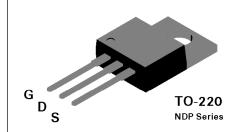
NDP6060L / NDB6060L N-Channel Logic Level Enhancement Mode Field Effect Transistor

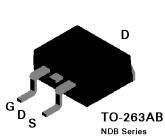
General Description

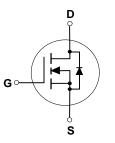
These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 48A, 60V. $R_{DS(ON)} = 0.025\Omega @ V_{GS} = 5V.$
- Low drive requirements allowing operation directly from logic drivers. V_{GS(TH)} < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







Absolute Maximum Ratings T_c = 25°C unless otherwise noted

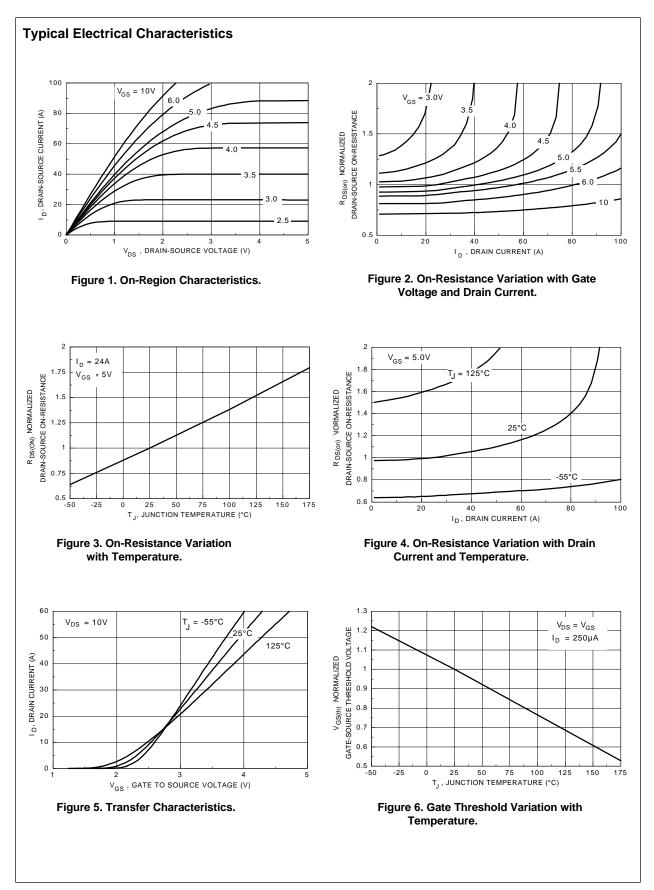
Symbol	Parameter	NDP6060L	NDB6060L	Units
V _{DSS}	Drain-Source Voltage	60		V
V _{dgr}	Drain-Gate Voltage ($R_{GS} \leq 1 M\Omega$)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive ($t_P < 50 \ \mu s$)	±25		
I _D	Drain Current - Continuous	48		А
	- Pulsed	144		
P _D	Total Power Dissipation @ $T_c = 25^{\circ}C$	100		W
	Derate above 25°C	0.67		W/°C
Γ _J ,T _{stg}	Operating and Storage Temperature	-65 to 17	°C	
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

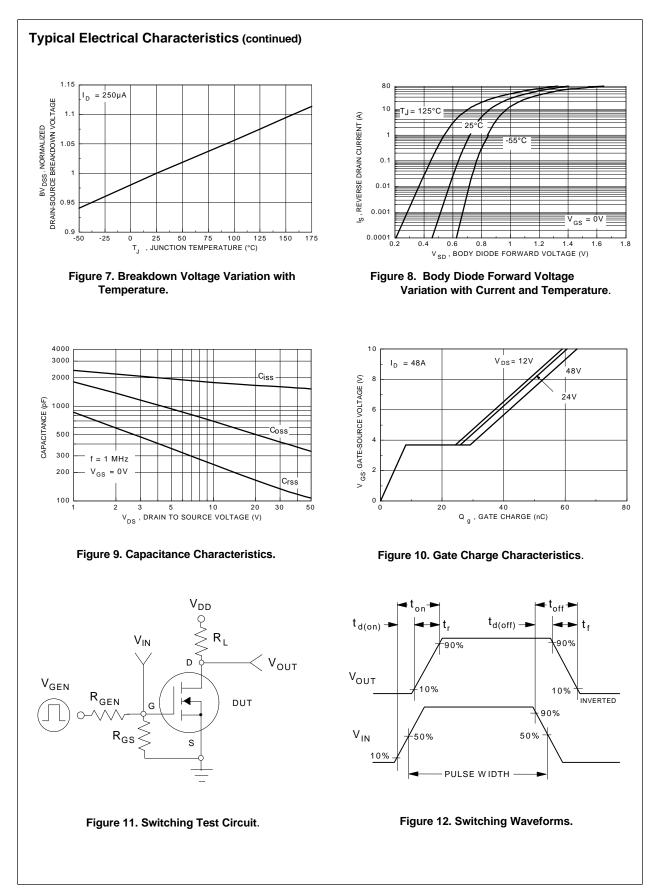
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Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)						
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, \text{ I}_{D} = 48 \text{ A}$				200	mJ
I _{AR}	Maximum Drain-Source Avalanche Cu	rrent				48	А
OFF CH/	ARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$		60			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$				250	μA
			T _J = 125°C			1	mA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$				-100	nA
ON CHAP	RACTERISTICS (Note 1)			•			
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$		1		2	V
			T _J = 125°C	0.65		1.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 5 \text{ V}, \text{ I}_{D} = 24 \text{ A}$				0.025	Ω
			T _J = 125°C			0.04	
		$V_{GS} = 10 \text{ V}, I_{D} = 24 \text{ A}$				0.02	
I _{D(on)}	On-State Drain Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$		48			А
9 _{FS}	Forward Transconductance	$V_{\rm DS} = 10 \text{ V}, I_{\rm D} = 24 \text{ A}$		10			S
DYNAMI	CCHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			1630	2000	pF
C _{oss}	Output Capacitance				460	800	pF
C _{rss}	Reverse Transfer Capacitance				150	400	рF
	NG CHARACTERISTICS (Note 1)				1		
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 30 \text{ V}, I_{D} = 48 \text{ A},$			15	30	nS
t,	Turn - On Rise Time	$V_{GS} = 5 \text{ V}, \text{R}_{GEN} = 15 \Omega,$ $\text{R}_{GS} = 15 \Omega$			320	500	nS
t _{D(off)}	Turn - Off Delay Time				49	100	nS
t _f	Turn - Off Fall Time				161	300	nS
 Q_	Total Gate Charge	$V_{DS} = 48 \text{ V},$ $I_{D} = 48 \text{ A}, V_{GS} = 5 \text{ V}$			36	60	nC
Q _{gs}	Gate-Source Charge				8.2		nC
Q _{gd}	Gate-Drain Charge	1			21		nC

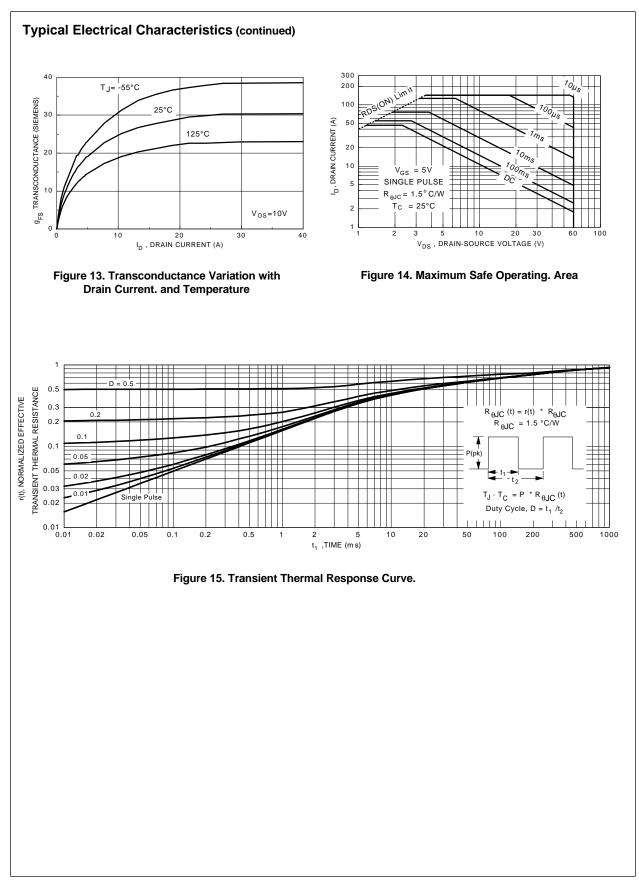
Electric	cal Characteristics (T _c = 25°C unle	ess otherwise noted)					
Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-SC	OURCE DIODE CHARACTERISTICS						
l _s	Maximum Continuos Drain-Source Diode Forward Current				48	А	
I _{SM}	Maximum Pulsed Drain-Source Diode Fo	orward Current				144	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{S} = 24 \text{ A}$ (Note 1)				1.3	V
			T _J = 125°C			1.2	
t _m	Reverse Recovery Time	$V_{GS} = 0 V, I_F = 48 A,$		35	75	140	ns
l _{rr}	Reverse Recovery Current	─ dl _F /dt = 100 A/µs		2	3.6	8	A
THERMA	L CHARACTERISTICS					•	
R _{θJC}	Thermal Resistance, Junction-to-Case					1.5	°C/W
R _{ØJA}	Thermal Resistance, Junction-to-Ambient				62.5	°C/W	

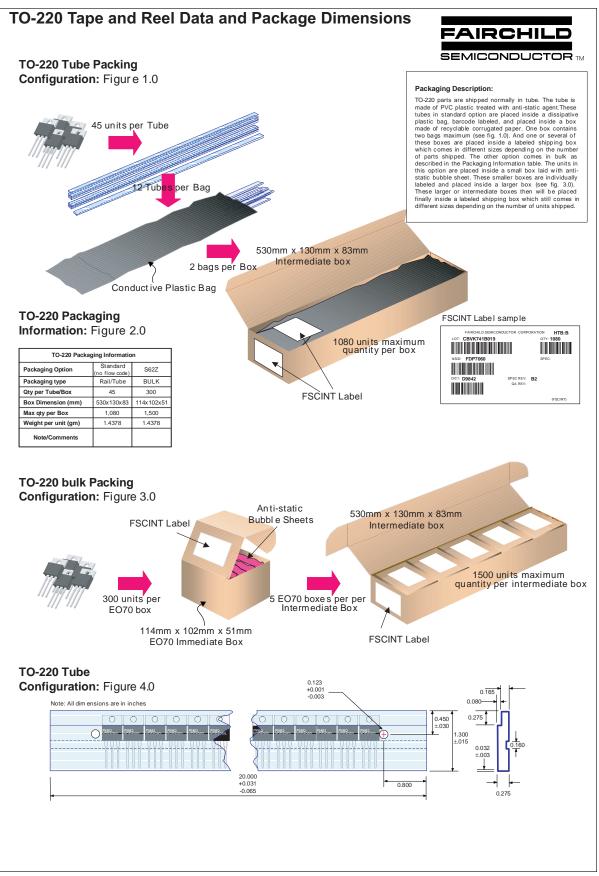
Note: 1. Pulse Test: Pulse Width \leq 300 µs, Duty Cycle \leq 2.0%.



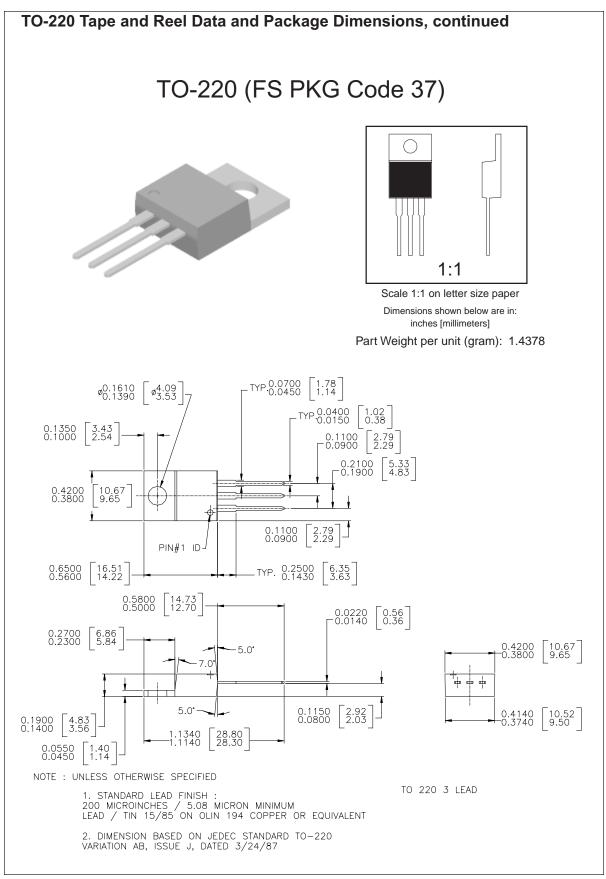


NDP6060L Rev. D / NDB6060L Rev. E

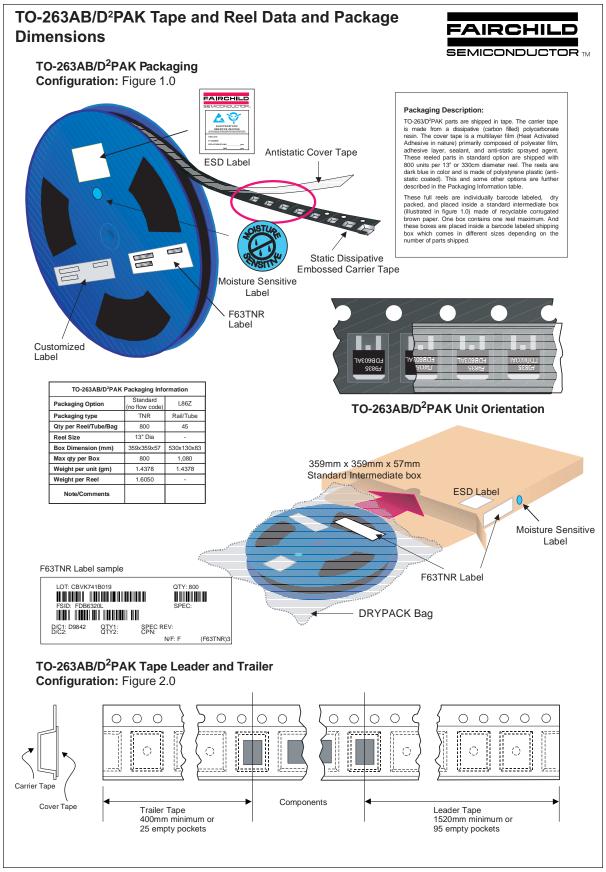




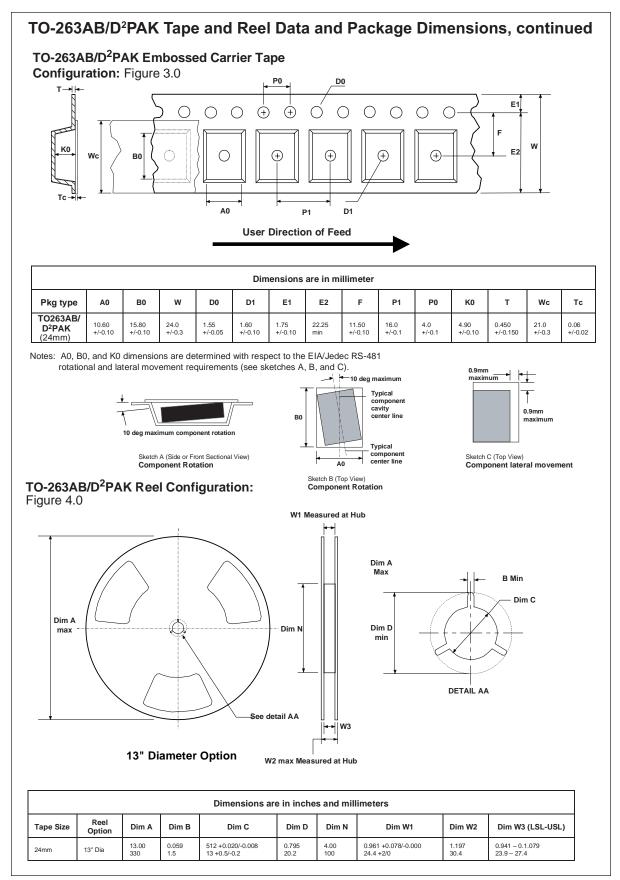
August 1999, Rev. B

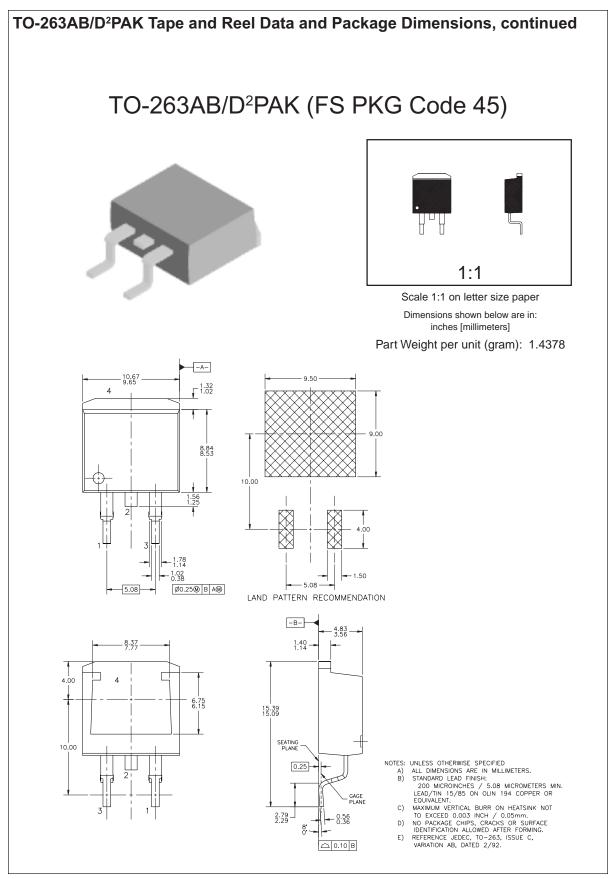


September 1998, Rev. A



September 1999, Rev. B





August 1998, Rev. A

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Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.				
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